

FEATURES AND BENEFITS

- ▶ Small footprint solution.
- ▶ 130A application with ultra low profile.
- ▶ Typical efficiency greater than 86%
- ▶ Proprietary control supports > 1200A/us step load transient response.
- ▶ Soft-start, current limiting under-voltage lockout and short circuit protection features included.
- ▶ Output Enable pin available.
- ▶ Change one external resistor to selected with VRM10.X, VRM11.
- ▶ SMBus for power manager.
- ▶ Change one external resistor to select output setpoint voltage.

APPLICATIONS

- ▶ CPU Power: Intel VRM10.X
Intel VRM11
- ▶ DSP Power Supplies
- ▶ Graphics Cards
- ▶ FPGAs
- ▶ Telecom Line Cards
- ▶ Datacom Equipment
- ▶ Broadband Communications ASICs
- ▶ General Purpose Point of Load Regulation

GENERAL DESCRIPTION

The AcBel 130A single output module is a new non-isolated high performance DC/DC converter designed to power advanced DSPs. This module provides a compact, highly efficient, fast, accurate, and reliable power delivery module for emerging low-output voltage applications.

OPERATION

The module is a high-frequency step-down switching regulator module optimized for application requiring small size, high efficiency, and low output voltages. The following sections describe specific features of the module in greater detail.



SPECIFICATIONS

Specification at 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{in}	Input Voltage Range	12Vdc +/-10%	10.8	12	13.2	V
I _{in}	Input Current Range	VID1.3625V /130A		15.3		A
V _{out}	Output VID Code Range	VRM10.X (VID_SEL=Open)	0.83125	1.325	1.6000	V
		VRM11 (VID_SEL=Open)	0.81875	1.3625	1.6000	
V _{SP}	Output Setpoint Voltage	VRM11	VID-15.625mV+SP			V
ΔV _{out}	Line Regulation	V _{in} =12Vdc +/-10% I _{out} =0A		2		mV
	Load Regulation	Load line (I _{out} =0A ~ 130A)	VID- (I _{out} *1.25mΩ)-30mV		VID- (I _{out} *1.25mΩ)	V
	Output Ripple (Static)	VRM10.X, VRM11			30	mVp-p
I _{cc} (TDC)	Output Current (Thermal design current)	VRM10.X			105	A
		VRM10.2			130	
		VRM11			130	
I _{cc} (Max)	Output Peak Current	VRM10.X			120	A
		VRM10.2 / VRM11			150	
OCP	Overcurrent Protection	VRM10.X, VRM11			180	A
Eff	Efficiency (Measured at inductor)	VID1.3625V I _{out} =100A		88.7		%
		VID1.3625V I _{out} =130A		87.3		
Top	Operating Temperature Range (Air-flow =400LFM)	VID1.200V I _{out} =130A	0		37.9	°C
		VID1.200V I _{out} =102.6A	0		50	
SR _{out}	Output Current Slew Rate (Based on C _{in} and C _{out})	VRM10.X	± 930			A/uS
		VRM10.2 / VRM11	± 1200			
C _{in}	Input Capacitance	MLCC: 10uF*3+ 1uF*3 + 0.1uF*12		34.2		u F
C _{out}	Output Capacitance	MLCC: 10uF *53 + 22uF *10		750		u F
VR_Ready	VRM is ready	Maximum voltage	0		3.6	V



VR6002-030G
Universal CPU Power Supply Module

Intel VRM10.X, VRM11
10.8~13.2Vdc Input

Symbol	Parameter	Condition	Min	Typ	Max	Units	
Vbias	Bias voltage for the VRM control	3.3Vdc	3.0	3.3	3.6	V	
SC	SMBus Clock Bus	Host input voltage	High	2.4		3.6	V
SD	SMBus Data Bus		Low	0		0.8	V
OE	Output Enable	Host input voltage	ON	0.9	3.3	3.6	V
			OFF	0		0.4	
VIDx	Voltage Identification (VID [6:0])	Input High Voltage	0.8		3.6	V	
		Input Low Voltage	0		0.4		
VID_SEL	VID Table Selection	VRM11	No stuff			ohm	
VR_HOT	Voltage Regulator Hot	Output High Voltage	2.4		Vbias	V	
		Output Low Voltage	0		0.4		
I_UVLO	Input Under Voltage	Resumes Normal Operation		8.91		V	
I_OVLO	Input Over Voltage	Resumes Normal Operation		9.69		V	
OVP	Oversvoltage Protection	Crowbar circuit		2.08		V	
SMBus	Communication with Processor	Advanced monitoring and control capabilities					
Tst	Storage Temperature range	Relative humidity <70%RH	5		35	°C	
*	Weight					g	
*	Size	L * W * T	96.5 * 64 * 17			mm	

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SMBus Interface Summary

Register Address (Command Code)	Name	Read/Write	Units	Description
30 (00011110)	Average Output Current	Read	N/A	Number representing the average system output current.
4 (00000100)	Maximum Output Current	Read	N/A	Number representing the maximum system output current based on current configuration.
5 (00000101)				
28 (00011100)	VID settings	Read	N/A	VID code settings.

SMBus Information

Average Output Current
Byte (Command Code 00010001)

B7	B6	B5	B4	B3	B2	B1	B0
sign	lavg6	lavg5	lavg4	lavg3	lavg2	lavg1	lavg0

1	0	1	38
1	1	0	34
1	1	1	30

The average output current =
 $\{(REG30[7:0])/126\} * (I_{max} \text{ value}) * (REG14[4:0])$

VID Code Settings

Byte (Command Code 00011100)

B7	B6	B5	B4	B3	B2	B1	B0
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0

VID code settings are read from register address 00011100.

Maximum Output Current
Byte (Command Code 00000100)

B7	B6	B5	B4	B3	B2	B1	B0
I1	I0	X	X	X	X	X	X

Byte (Command Code 00000101)

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	X	X	I2

Note: The I_{max} Values are given in the following table:

I2	I1	I0	I _{max} Value
0	0	0	24
0	0	1	36
0	1	0	32
0	1	1	28
1	0	0	26

MECHANICAL DRAWING

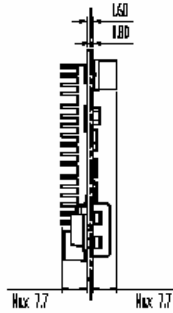
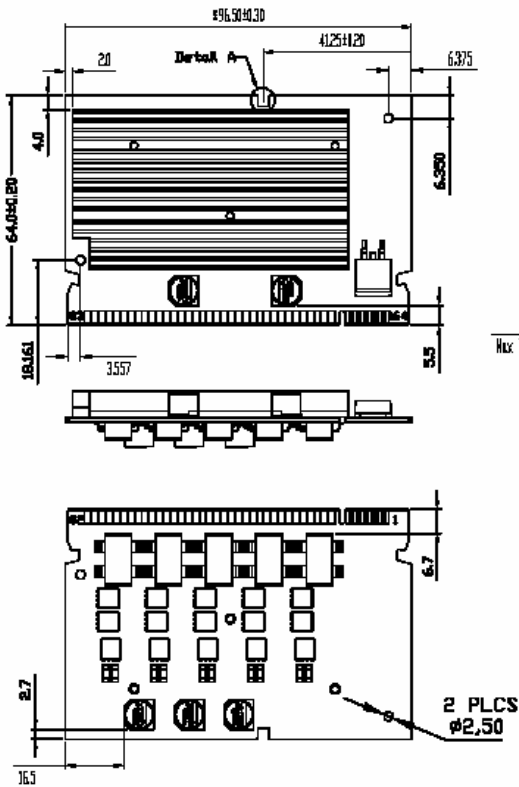
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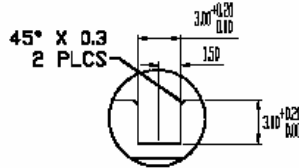
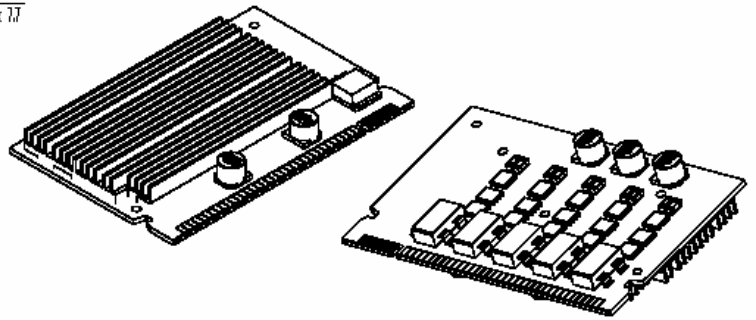
Intel VRM10.X, VRM11
10.8~13.2Vdc Input



NOTE:

- 1.UNIT:MM
- 2.TOLERANCE= ±0.25
- 3.BASE ON IBM SPEC.HIGH EFFICIENCY 2U,130A,7 VID VRM11 FOR CPU APPLICATION.

4.VRM CONTACT CONNECTOR: USE MOLEX 87787-1011 OR 87786-1011.



Detail A;Scale 4:1

Pin-Out Assignment

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VR6002-030G
Universal CPU Power Supply Module

Intel VRM10.X, VRM11
10.8~13.2Vdc Input

Front Side		Back Side	
Pin	Description	Pin	Description
1	VR_Ready	164	Vbias
2	SC	163	SD
3	OE	162	LL0
4	LL1	161	VID6
5	VID5	160	VID4
6	VID3	159	VID2
7	VID1	158	VID0
8	Spare	157	Spare
9	Vsense +	156	Vsense -
10	SP	155	VID SEL
11	VR_HOT	154	VRM_Pres
12	VR_FAN	153	Bus_ADD
Key			
13,14,15,16	VIN+	149,150,151,152	VIN+
17,18,19,20	GND	145,146,147,148	GND
21,22,23,24	VO+	141,142,143,144	VO+
25,26	GND	139,140	GND
27,28,29,30	VO+	135,136,137,138	VO+
31,32,33,34	GND	131,132,133,134	GND
35,36,37,38	VO+	127,128,129,130	VO+
39,40,41,42	GND	123,124,125,126	GND
43,44,45,46	VO+	119,120,121,122	VO+
47,48	GND	117,118	GND
49,50,51,52	VO+	113,114,115,116	VO+
53,54,55,56	GND	109,110,111,112	GND
57,58,59,60	VO+	105,106,107,108	VO+

Pin	Description	Pin	Description
61,62,63,64	GND	101,102,103,104	GND
65,66,67,68	VO+	97,98,99,100	VO+
69,70	GND	95,96	GND
71,72,73,74	VO+	91,92,93,94	VO+
75,76,77,78	GND	87,88,89,90	GND
79,80,81,82	VO+	83,84,85,86	VO+

Front Side	Back Side
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Pin-Out Signal Name Definitions

VR_Ready (Pin 1)

The VR_Ready pin is an open collector signal to indicate the regulator output voltage is within the specified range. The pull-up resistor and voltage source shall be located on the baseboard.

“1”...uP VCC within 10% of target regulation voltage.

“0”...uP VCC outside 10% of target regulation voltage.

SC (Pin 2)

The SC pin provides an SMBus clock connection to the VRM. The pull-up resistor and voltage source shall be located on the baseboard.

OE (Pin 3)

The Output Enable pin is used to enable or disable the output voltage. It is an open collector signal. The pull-up resistor and voltage source shall be located on the baseboard.

“1”... Regulator output enabled.

“0”... Regulator output disabled.

LL1, LL0 (Pin 4, 162)

The host will use these signals to control output voltage droop.

VID0, 1, 2, 3, 4, 5, 6 (Pin 158, 7, 159, 6, 160, 5, 161)

Voltage Identification input pins. These pins are used to program the VRM output voltage. Voltage programming is achieved by pulling these pins LOW or HIGH. Detail VID table see the Table1, Table2.

Spare (Pin 8, 157)

These Spare pins for the advance used in the future.

Vsense+ (Pin 9)

The Vsense+ is positive end of the output voltage remote sense. This pin should be connected to the remote sense point at the desired remote regulation point.

VR_HOT (Pin 11)

This pin will remain low level as long as the VRM temperatures are above the thermal threshold point and de-assert to high when temperatures cool below the threshold point. The temperature threshold hysteric is designed.

VR_PAN (Pin 12)

This pin will remain high as long as temperatures are above the threshold point and de-assert to low when temperatures cool below the threshold point. Threshold hysteric is designed.

Bus_ADD (Pin 153)

The Bus_ADD signal combined with the VRM_present signal forms a two-bit VRM identification code to indicate the type of module installed in a system.

Table 3 defines the two signal decode.

VRM_Pres (Pin 154)

The VRM present pin is an output signal used to indicate to the system that a VRM 10.X compatible module is plugged into the socket.

Table 3 defines the signal decode.

VID SEL (Pin 155)

The VID select pin can be choosing. VID table selection input.

“1”... VRM11 VID table selected.

“0”... VRM10 VID table selected.

Detail VID table see the Table1, Table 2.

Vsense - (Pin 156)

The Vsense- pin is the negative end of the output voltage remote sense. This pin should be connected to the GND plane at the desired remote regulation point.

SD (Pin 163)

This pin provides an SMBus data signal connection to the VRM. The pull-up resistor and voltage source shall be located on the baseboard.

Vbias (Pin 164)

This pin provides 500mA maximum of 3.3V \pm 7% for all sequence and control logic, including the serial bus.

VO+

Pins (P21-P24, P27-P30, P35-P38, P43-P46, P49-52, P57-P60, P65-P68, P71-P74, P79-P86, P91-P94, P97-P100, P105-P108, P113-P116, P119-P122, P127-130, P135-P138, P141-P144): Output voltage supply.

VIN+

Input voltage pins. Pins (P13-P16, P149-P152): These pins connect directly to the input power supply source.

GND

Pins (P17-P20, P25, P26, P31-P34, P39-P42, P47, P48, P53-P56, P61-P64, P69, P70, P75-P78, P87-P90, P95, P96, P101-P104, P109-P112, P117, P118, P123-P126, P131-P134, P139, P140, P145-P148): Input / Output voltage ground.



Table 1: Intel VRM 10.X

VID _{HI} (hex)	VID _{LO} (hex)	Voltage (V)	VID _{HI} (hex)	VID _{LO} (hex)	Voltage (V)	VID _{HI} (hex)	VID _{LO} (hex)	Voltage (V)
2	B	1.60000	5	4	1.33125	0	1	1.08750
2	A	1.59375	5	7	1.32500	0	0	1.08125
2	D	1.58750	5	6	1.31875	0	3	1.07500
2	C	1.58125	5	9	1.31250	0	2	1.06875
2	F	1.57500	5	8	1.30625	0	5	1.06250
2	E	1.56875	5	B	1.30000	0	4	1.05625
3	1	1.56250	5	A	1.29375	0	7	1.05000
3	0	1.55625	5	D	1.28750	0	6	1.04375
3	3	1.55000	5	C	1.28125	0	9	1.03750
3	2	1.54375	5	F	1.27500	0	8	1.03125
3	5	1.53750	5	E	1.26875	0	B	1.02500
3	4	1.53125	6	1	1.26250	0	A	1.01875
3	7	1.52500	6	0	1.25625	0	D	1.01250
3	6	1.51875	6	3	1.25000	0	C	1.00625
3	9	1.51250	6	2	1.24375	0	F	1.00000
3	8	1.50625	6	5	1.23750	0	E	0.99375
3	B	1.50000	6	4	1.23125	1	1	0.98750
3	A	1.49375	6	7	1.22500	1	0	0.98125
3	D	1.48750	6	6	1.21875	1	3	0.97500
3	C	1.48125	6	9	1.21250	1	2	0.96875
3	F	1.47500	6	8	1.20625	1	5	0.96250
3	E	1.46875	6	B	1.20000	1	4	0.95625
4	1	1.46250	6	A	1.19375	1	7	0.95000
4	0	1.45625	6	D	1.18750	1	6	0.94375
4	3	1.45000	6	C	1.18125	1	9	0.93750
4	2	1.44375	6	F	1.17500	1	8	0.93125
4	5	1.43750	6	E	1.16875	1	B	0.92500
4	4	1.43125	7	1	1.16250	1	A	0.91875
4	7	1.42500	7	0	1.15625	1	D	0.91250
4	6	1.41875	7	3	1.15000	1	C	0.90625
4	9	1.41250	7	2	1.14375	1	F	0.90000
4	8	1.40625	7	5	1.13750	1	E	0.89375
4	B	1.40000	7	4	1.13125	2	1	0.88750
4	A	1.39375	7	7	1.12500	2	0	0.88125
4	D	1.38750	7	6	1.11875	2	3	0.87500
4	C	1.38125	7	9	1.11250	2	2	0.86875
4	F	1.37500	7	8	1.10625	2	5	0.86250
4	E	1.36875	7	B	1.10000	2	4	0.85625
5	1	1.36250	7	A	1.09375	2	7	0.85000
5	0	1.35625	7	D	OFF	2	6	0.84375
5	3	1.35000	7	C	OFF	2	9	0.83750
5	2	1.34375	7	F	OFF	2	8	0.83125
5	5	1.33750	7	E	OFF			

Notes:VID_{HI} = (VID4, VID3, VID2), VID_{LO} = (VID1, VID0, VID5, VID6)

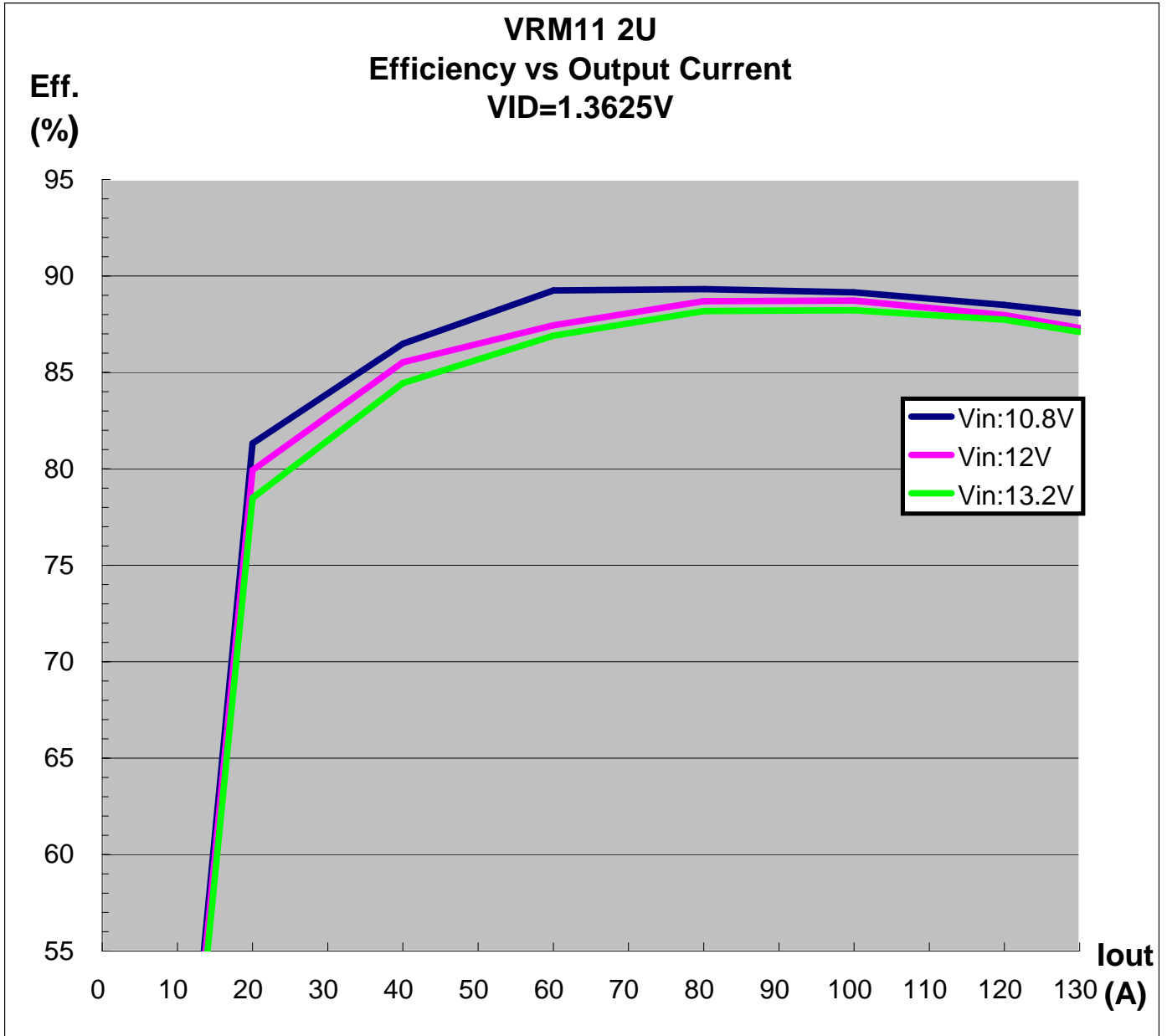
VID[6] must be set high for standard VRM 10.X VID codes.



Table 2: Intel VRM 11

VID _{HI} (hex)	VID _{LO} (hex)	Voltage (V)	VID _{HI} (hex)	VID _{LO} (hex)	Voltage (V)	VID _{HI} (hex)	VID _{LO} (hex)	Voltage (V)
0	0	OFF	2	C	1.33750	5	8	1.06250
0	1	OFF	2	D	1.33125	5	9	1.05625
0	2	1.60000	2	E	1.32500	5	A	1.05000
0	3	1.59375	2	F	1.31875	5	B	1.04375
0	4	1.58750	3	0	1.31250	5	C	1.03750
0	5	1.58125	3	1	1.30625	5	D	1.03125
0	6	1.57500	3	2	1.30000	5	E	1.02500
0	7	1.56875	3	3	1.29375	5	F	1.01875
0	8	1.56250	3	4	1.28750	6	0	1.01250
0	9	1.55625	3	5	1.28125	6	1	1.00625
0	A	1.55000	3	6	1.27500	6	2	1.00000
0	B	1.54375	3	7	1.26875	6	3	0.99375
0	C	1.53750	3	8	1.26250	6	4	0.98750
0	D	1.53125	3	9	1.25625	6	5	0.98125
0	E	1.52500	3	A	1.25000	6	6	0.97500
0	F	1.51875	3	B	1.24375	6	7	0.96875
1	0	1.51250	3	C	1.23750	6	8	0.96250
1	1	1.50625	3	D	1.23125	6	9	0.95625
1	2	1.50000	3	E	1.22500	6	A	0.95000
1	3	1.49375	3	F	1.21875	6	B	0.94375
1	4	1.48750	4	0	1.21250	6	C	0.93750
1	5	1.48125	4	1	1.20625	6	D	0.93125
1	6	1.47500	4	2	1.20000	6	E	0.92500
1	7	1.46875	4	3	1.19375	6	F	0.91875
1	8	1.46250	4	4	1.18750	7	0	0.91250
1	9	1.45625	4	5	1.18125	7	1	0.90625
1	A	1.45000	4	6	1.17500	7	2	0.90000
1	B	1.44375	4	7	1.16875	7	3	0.89375
1	C	1.43750	4	8	1.16250	7	4	0.88750
1	D	1.43125	4	9	1.15625	7	5	0.88125
1	E	1.42500	4	A	1.15000	7	6	0.87500
1	F	1.41875	4	B	1.14375	7	7	0.86875
2	0	1.41250	4	C	1.13750	7	8	0.86250
2	1	1.40625	4	D	1.13125	7	9	0.85625
2	2	1.40000	4	E	1.12500	7	A	0.85000
2	3	1.39375	4	F	1.11875	7	B	0.84375
2	4	1.38750	5	0	1.11250	7	C	0.83750
2	5	1.38125	5	1	1.10625	7	D	0.83125
2	6	1.37500	5	2	1.10000	7	E	0.82500
2	7	1.36875	5	3	1.09375	7	F	0.81875
2	8	1.36250	5	4	1.08750			
2	9	1.35625	5	5	1.08125			
2	A	1.35000	5	6	1.07500			
2	B	1.34375	5	7	1.06875			

Efficiency Curve



NOTE: Vout Measured at inductor